SAULT COLLEGE OF APPLIED ARTS & TECHNOLOGY

SAULT STE. MARIE, ONTARIO

COURSE OUTLINE

Course Title: DIGITAL ELECTRONICS

Code No.: ELN 107-5

Program: ELECTRICAL/ELECTRONIC TECHNICIAN

Semester: TWO

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APPROVED: L.P. Arezzitto
Chairperson

Date

LOGIC & SWITCHING CIRCUITS

ELN 107

NUMBER OF THEORY PERIODS: 28
NUMBER OF LABORATORY PERIODS: 21

PREREQUISITES: ELN 100, Electronic I

TEXTBOOKS: Digital Fundamentals (2nd Ed.), by Thomas L. Floyd

National Logic Data Book

BLOCKS	THEORY PERIODS	TOPIC DESCRIPTION	REFERENCE CHAPTERS
I	9	Logic Gates and Combinational Logic Boolean Algebra	1, 2, 3, 5, A
II	7	Integrated Circuit Technologies Functions of Combinational Logic	A 6
III	9	Flip-Flops, Counters and Registers	7, 8
IV	3	Interfacing and Data Transfer	10

OBJECTIVES

BLOCK I:	THEORY PERIODS
Introduction: Logic levels and pulse waveforms Logic functions, elements of digital logic	1
Logic Gates: The INVERTER, AND, OR, NAND, NOR gates. Truth tables. Integrated circuit parameters	3
Boolean Algebra: Applications: logic expressions. Simplification of Boolean expressions	1
Combinational Logic: Analysis, implementation and simplification of logic networks. Enable and inhibit operation. The universal property of the inverting gates (NAND, NOR). The AND-OR- INVERT gate operation. Exclusive OR and exclusive NOR.	3
BLOCK TEST	1
BLOCK II:	
Integrated Circuit Technologies: TTL versus CMOS. Low power, Scmottky, ECL, I^2L logic	2
Functions of Combinational Logic: Parallel binary adders; comparators; decoders - encoders; multiplexers - demultiplexers; parity generators - checkers	4
BLOCK TEST	1
BLOCK III:	
Flip-Flops: S-R Latches - cross-coupled NAND - cross-coupled NOR D Latch Edge triggered S-R Flip-Flop Master-Slave S-R Flip-Flop Edge triggered D Flip-Flop J-K Flip-Flops Electrical and Switching Characteristics One-Shot (Monostable) Multivibrator	3

Counters:	Binary Counters Decade Counters Asynchronous Counters Synchronous Counters Up-Down Synchronous Counters Cascaded Counters	4
Shift Registers:	Serial in - serial out registers Parallel in - serial out registers Serial in - parallel out registers Parallel in - parallel out Bidirectional shift registers	2

BLOCK IV:

Interfacing and Data Transfer:	Three state buffer The Schmitt trigger Digital to analog conversion Analog to digital conversion	2
BLOCK TEST (III & IV)		1

SPECIFIC OBJECTIVES

BLOCK I: Logic Gates and Combinational Logic

At the end of this block, the student will be able to:

1) Distinguish an analog and a digital signal.
2) Recall the meaning of the positive and negative logic, high and low level, leading and trailing edge of a digital signal.
3) Represent digital information in serial and parallel form with waveforms. Identify MSB and LSB.
4) Recall nonideal pulse characteristics and waveforms.
5) Draw logic symbols and truth tables for NOT, AND, NAND, OR, NOR operation.
6) Analyse TTL and CMOS logic gate circuit diagrams.
7) Recall logic gate parameters: unit load, fan out, input and output voltage level, input and output current, noise margin, supply current, turn on delay, turn-off delay, gate propagation delay and operating frequence.
8) Given a logic diagram, write and simplify the corresponding Boolean equation.
9) Given a Boolean equation, produce a logic diagram using specified types of gates to implement the equation.
10) Use logic gates to enable or inhibit the passage of digital signals.
11) Based on the universal property of the inverting gates, generate AND, NAND, OR, NOR functions with both NAND gate NOR gate.
12) Write the Boolean equation and draw the logic symbol of the AND-OR-INVERT operation.
13) Produce the truth table and the symbol of the exclusive OR and exclusive NOR gates.
14) Manipulate Boolean equations of logic diagrams including exclusive gates.

BLOCK II: Integrated Circuit Technologies

At the end of this block, the student will be able to:

15) Discuss power and speed characteristics of modern digital circuits, and describe the special tecniques used for high speed operation (Scmottky, ECL, I^2L).
16) Identify integrated circuits by the designated series number: (54/74; 54L/74L; 54M/74M; 54S/74S; 54LS/74LS).
17) Describe the use of open collector gates and wired logic functions.
18) Describe the use of tree state gates.

Functions of Combinational Logic

19) Use logic gates to produce a binary half adder and full adder. Recall truth table for the half adder and the full adder.
20) Draw the block diagram of a multibit binary adder.

21) Use integrated circuit two bit and four bit adders to generate multibit adders.
22) Use exclusive OR gates to produce multibit parallel comparators.
23) Use integrated circuit four bit comparators to generate multibit parallel comparators.
24) Use logic gates to decode binary information.
25) Use integrated circuit 4 line to 16 line decoder and BCD decoder.
26) Use decoders like in-line readout drivers.
27) Use binary to 7 segment decoders.
28) Discuss the typical display techniques used with digital systems.
29) Recall the principle of encoding. Use integrated circuit decimal to BCD encoder.
30) Use logic gates for a four input multiplexer and a four line demultiplexer.
31) Describe and discuss integrated circuit multiplexers and demultiplexers.
33) Use integrated circuit parity generator/checker.

BLOCK III:

At the end of this block, the student will be able to:

Flip-Flops

34) Recall the logic diagram, logic symbols, truth tables and functional operation of the following type of flip-flops:

- set-reset crossed coupled NAND
- set-reset crossed coupled NOR
- D latch
- edge triggered set-reset flip-flop
- edge triggered D flip-flop
- master-slave S-R flip-flop
- J-K flip-flop.

35) Analyse and draw timing diagrams for the above flip-flops.
36) Use TTL data books to find electrical and switching characteristics of integrated circuit flip-flops.
37) Recall the logic diagrams, logic symbols and functional operations of integrated circuit one-shot monostable multivibrators.

Counters

38) Utilize standard flip-flops and gates to implement:

- asynchronous counters
- synchronous counters
- binary counters
- decade counters
- modulus N counters
- up-down counters

39) Use integrated circuit TTL four bit binary ripple counter for divide by N frequence divider.
40) Use cascaded counters for frequence divider.
41) Discuss and use integrated circuit four bit synchronous counters.
42) Discuss the digital clock like counter application.
43) Describe the operation of, and utilize standard flip-flops and gates to implement the following types of shift registers:

- serial in - serial out
- parallel in - serial out
- serial in - parallel out
- parallel in - parallel out
- shift right - shift left

44) Discuss and use integrated circuit four bit registers.

BLOCK IV: Interfacing and Data Transfer

At the end of this block, the student will be able to:

45) Use three state gates to interface digital devices to a bus.
46) Discuss bidirectional three State bus drivers.
47) Use the Schmitt trigger as an interface circuit.
48) Recall the operation and applications of D/A and A/D converters.
49) Recall the operation of a four bit binary weighted input D/A converter and of a four bit ladder D/A converter.
50) Recall the operation of the simultaneous, stair step ramp and tracking A/D converter.

LABORATORY ACTIVITY

JOB 1 - Logic Gates
- to reinforce specific objectives 5, 6, 7, 8, 11

JOB 2 - Combinational Logic
- to reinforce specific objectives 9, 10, 11, 12

JOB 3 - Combinational Logic Functions
- to reinforce specific objectives 25, 26, 27, 28, 31

JOB 4 - Flip-Flops
- to reinforce specific objectives 34, 35, 36

JOB 5 - Counters
- to reinforce specific objectives 39, 40, 41, 42

JOB 6 - Shift Registers
- to reinforce specific objectives 43, 44

JOB 7 - A/D and D/A Converters
- to reinforce specific objectives 48, 49, 50